REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claim 5 is cancelled.

Claims 1, 12, 14, 16, 18, 20, 21 and 22 are currently being amended.

This amendment changes and deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1, 6-18 and 20-22 are now pending in this application.

Claim Objections

Claim 16 was objected to for informalities. In response, Applicant has amended claim 16 to correct the informalities. Accordingly, Applicant requests that the objection be withdrawn.

Claim Rejections under 35 U.S.C. § 112

Claims 1, 5-18 and 20-22 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. In response, without agreeing or acquiescing to the rejection, Applicant has amended claims 1, 12, 14, 16, 18, 20 and 21 to comply with the written description requirement.

The Office Action states that the following limitations is not present in the original disclosure:

"a plurality of program data memories, each holding a program that creates a logic circuit directly in said reconfigurable hardware for each of said processing units,"

"said program is given control flow of the application program, completion data, structural information of the electronic computer and a plurality of command sets of the electronic computer as inputs;"

"said program executes a command sequence implementation procedure for translating said command sequence intermediate code into a data string that can be executed by the control device;"

Applicant respectfully disagrees. The limitation "a plurality of program data memories, each holding a program that creates a logic circuit directly in said reconfigurable hardware for each of said processing units" was originally disclosed at least in claim 3 of the application as filed. The limitations "said program is given control flow of the application program, completion data, structural information of the electronic computer and a plurality of command sets of the electronic computer as inputs" and "said program executes a command sequence implementation procedure for translating said command sequence intermediate code into a data string that can be executed by the control device" were originally disclosed at least in claim 16 of the application as filed.

Claims 1, 5-11, 14-18 and 20-22 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In response, without agreeing or acquiescing to the rejection, Applicant has amended claims 1, 12, 14, 16, 18, 20, 21 and 22 to adhere to the requirements under 35 U.S.C. § 112, second paragraph. In addition, Applicant directs the Examiner's attention to Figure 19 and ¶¶ [0019] – [0121] which explain how the claimed program is executed. Accordingly, Applicant requests that the rejection be withdrawn and claims 1, 6-11, 14-18 and 20-22 be allowed.

Claim Rejections under 35 U.S.C. § 102

Claim 18 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,658,564 ("Smith"). In response, without agreeing or acquiescing to the rejection,

Applicant has cancelled claim 5 and amended independent claim 18. Further, Applicant respectfully traverses the rejection for the reasons set forth below.

Applicant relies on M.P.E.P. § 2131, entitled "Anticipation – Application of 35 U.S.C. § 102(a), (b) and (e)" which states, "a claim is anticipated only if each and every element set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Applicant respectfully submits that Smith does not describe each and every element of the claims.

Claim 18 is directed to a program generation method for an electronic computer executing an application program divided into a plurality of processing units, wherein said electronic computer includes a processing device with reconfigurable hardware that can create a logic circuit for each of said processing units and a control device, comprising in addition to other elements "interpreting and executing: an activate command selecting one of said program data memories and activating said processing element to start processing a program held in one of the selected program data memories; a halt command halting operation of said processing device; a load_prg command transferring program data from a specified memory device to one of said program data memories, wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored; a cancel_prg command canceling a load_prg instruction, and a wait_prg command waiting until completion of the load_prg instruction."

Without limitation to the claims, Applicant directs the Examiner to Fig. 5. The control device 60 receives the command signal S41 sent from a device external to the electronic computer 30 via the interface device 40 and the command signal S91 outputted from the processing device 70, interprets, and executes the received command. An example of a protocol when the processing device 70 issues the command signal S91 to the control device 60 is shown in FIG. 6. This protocol may be applied as a protocol between the interface device 40 and the control device 60. An example of the command code that the control device 60 interprets and executes is shown in FIGS. 7 and 8. FIG. 7 is a diagram showing the structure of the command code, and a command code A 10 is made up of a

command code name All and a command code parameter A 12. FIG. 8 is a table showing the execution contents of commands and shows six commands.

In contrast, Smith does not disclose, teach or suggest each and every element recited in amended independent claim 18. Smith discloses a reconfigurable computer system. Smith discloses partitioning an application into blocks. *See* Col. 2, lines 4-8. Smith discloses that a partitioner automatically partitions a specification written in the system design language into software and hardware functions. *See* Col. 2, lines 24-26. However, Smith fails to disclose "interpreting and executing: an activate command selecting one of said program data memories and activating said processing element to start processing a program held in one of the selected program data memories; a halt command halting operation of said processing device; a load_prg command transferring program data from a specified memory device to one of said program data memories, wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored; a cancel_prg command canceling a load_prg instruction, and a wait_prg command waiting until completion of the load_prg instruction" as claimed in amended independent claim 18.

M.P.E.P. § 2131 states that"[t]he identical invention must be shown in as complete detail as is contained in the...claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *See In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Here, Smith fails to disclose each and every limitation in as complete detail as is contained in amended independent claim 18.

Accordingly, Applicant respectfully requests that the rejection be withdrawn and claim 18 be allowed. If this rejection of the claims is maintained, the examiner is respectfully requested to point out where the above-mentioned features are disclosed in Smith.

Claim Rejections under 35 U.S.C. § 103

Claims 1, 5, 15-17 and 21-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,326,806 ("Fallside") in view of Smith in view of U.S. Patent No. 6,288,566 ("Hanrahan"). Claims 12, 14 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fallside in view of Smith. Claims 6 and 7 were rejected

under 35 U.S.C. § 103(a) Fallside, Smith and Hanrahan and in further in view of U.S. Patent No. 5,887,189 ("Birns"). Claims 8 and 9 were rejected under 35 U.S.C. § 103(a) Fallside, Smith, Hanrahan, Birns and further view of U.S. Patent No. 5,473,763 ("Stewart"). Claims 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fallside, Smith and Hanrahan in view of U.S. Patent No. 4,860,192 ("Sachs"). In response, without agreeing or acquiescing to the rejection, Applicant has cancelled claim 5 and amended independent claims 1, 12, 14, 16, 20 and 21. Further, Applicant respectfully traverses the rejection for the reasons set forth below.

Applicant relies on MPEP § 2143.03, which requires that all words in a claim must be considered in judging the patentability of that claim against the prior art. Here, the cited references do not identically disclose, teach or suggest all the claim limitations. *See In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Claims 1 and 12 are directed to an electronic computer having a program for dividing an application into a plurality of processing units and generating program data and command code sequences. Claims 14 and 16 are directed to a control method for an electronic computer. Claims 20 and 21 are directed to a computer program product for an electronic computer which when executed performs a method implemented using reconfigurable hardware.

Specifically, the above claims require a method and a processing device including a program for dividing an application into a plurality of processing units and generating program data and command code sequences executed by said electronic computer, said electronic computer comprising a processing device and a control device. The control device "interprets and executes: an activate command selecting one of said program data memories and activating said processing element to start processing a program held in one of the selected program data memories; a halt command halting operation of said processing device; a load_prg command transferring program data from a specified memory device to one of said program data memories, wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored; a cancel_prg

command canceling a load_prg instruction, and a wait_prg command waiting until completion of the load_prg instruction."

Without limitation to the claims, Applicant directs the Examiner to Fig. 5. The control device 60 receives the command signal S41 sent from a device external to the electronic computer 30 via the interface device 40 and the command signal S91 outputted from the processing device 70, interprets, and executes the received command. An example of a protocol when the processing device 70 issues the command signal S91 to the control device 60 is shown in FIG. 6. This protocol may be applied as a protocol between the interface device 40 and the control device 60. An example of the command code that the control device 60 interprets and executes is shown in FIGS. 7 and 8. FIG. 7 is a diagram showing the structure of the command code, and a command code A 10 is made up of a command code name All and a command code parameter A 12. FIG. 8 is a table showing the execution contents of commands and shows six commands.

Fallside, Smith and Hanrahan do not disclose, teach or suggest each and every element of independent claims 1, 12, 14, 16, 18, 20 and 21. Fallside is directed to a FPGA-Based system. Pages 27-28 of the Office Action assert that Fallside discloses all the limitations of cancelled claim 5. However, Fallside fails to disclose, teach or suggest "an activate command selecting one of said program data memories and activating said processing element ***to start processing a program held in one of the selected program data memories***" and "a load_prg command transferring program data from a specified memory device to one of said program data memories, ***wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored***."

Further, Birns, Stewart, Sachs fail to cure the deficiencies of Fallside, Smith and Hanrahan. Accordingly, Applicant respectfully request that the rejection be withdrawn and independent claims 1, 12, 14, 16, 18, 20 and 21 be allowed. Further, claims 3,4, 6-11, 13, 15, 17 and 22 depend from one of independent claims 1, 12, 14, 16, 20 and 21 and should therefore be allowable for the reasons set forth above without regard to further patentable limitations cited therein.

If this rejection of the claims is maintained, the examiner is respectfully requested to point out where the above-mentioned features are disclosed in Fallside, Smith, Hanrahan, Birns, Stewart or Sachs.

Conclusion

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date 2/29/09

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